UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,555	03/12/2004	Tadashi Yamaguchi	OKI 413	6470

7590 03/20/2006

RABIN & BERDO, P.C.
Suite 500
1101 14th Street
Washington, DC 20005

EXAMINER	
MATISIAK, JENNIFER E	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,555	YAMAGUCHI, TADASHI	
	Examiner	Art Unit	
	Jennifer Matisiak	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4 and 9 is/are rejected.

7)☒ Claim(s) 5-8 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 03012200[illegible]
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

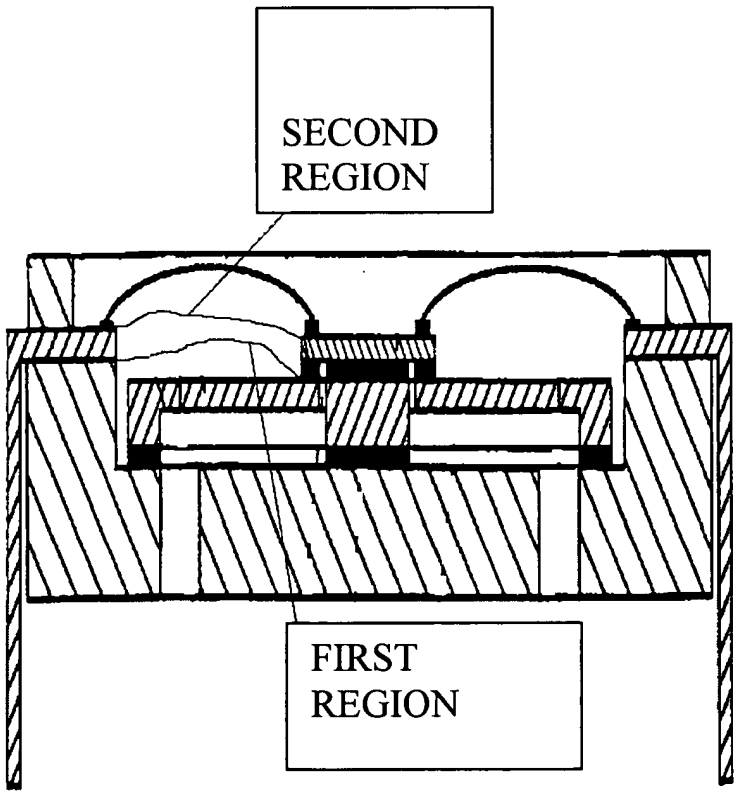
> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-4 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Benavides et al (US 6548895), hereinafter Benavides.

Regarding claim 1, Benavides discloses a semiconductor device (Fig. 11, for example) comprising: a semiconductor chip (100) having a first main surface and a second main surface opposite to the first main surface; a mounting substrate (40) having a chip mounting surface (44) which has an area wider than an area of the second main surface and is opposed face to face with the second main surface, said mounting substrate having chip mounted thereon; an encapsulating layer (col 13, lines 4-6) formed on the chip mounting surface (44) so as to cover the semiconductor chip; wiring patterns (104) electrically connected to the electrode pads and extending from above a first region (see figure below) located above the semiconductor chip, of an internal surface region of the encapsulating layer to above a second region (see figure below) that surrounds the first region; and external terminals (58) disposed on, where "on" is interpreted to mean "in contact with," the surfaces of the wiring patterns located

on the second region, wherein trenches (54) extending between a pair of opposite side surfaces of the mounting substrate are defined in the chip mounting surface of the mounting substrate, and the encapsulating layer is formed in the trenches (col 13, lines 4-6).

While does Benavides not explicitly state, "formed with electrode pads," the invention of Benavides inherently includes electrode pads since it is required for the chip to facilitate external communication with other devices.



Regarding claim 2, Benavides discloses a semiconductor device wherein the semiconductor chip is mounted on the mounting substrate along, where "along" is interpreted as meaning "in the direction of," the trenches (Fig. 11).

Regarding claim 3, Benavides discloses a semiconductor device wherein the semiconductor chip is mounted on the mounting substrate in alignment with the trenches (Fig. 11).

Regarding claim 4, Benavides discloses a semiconductor device wherein the semiconductor chip is mounted on the mounting substrate with being spaced a predetermined distance from the trenches respectively (Fig. 11).

Regarding claim 9, Benavides discloses a semiconductor device (Fig. 11) comprising: semiconductor chip (100) having a first main surface formed with electrode pads (102) and a second main surface opposite to the first main surface; a mounting substrate (40) having a chip mounting surface (44) which has an area wider than an area of the second main surface (see figure above) and is opposed face to face with the second main surface, said mounting substrate having the semiconductor chip mounted thereon; an encapsulating layer (col 13, lines 4-6) formed on the chip mounting surface so as to cover the semiconductor chip; wiring patterns (104) electrically connected to the electrode pads and extending from above a first region located (see figure above) above the semiconductor chip, of an internal surface region of the encapsulating layer to above a second region (see figure above) that surrounds the first region; and external terminals (58) disposed on, where "on" is interpreted to mean "in contact with," the surfaces of the wiring patterns located on the second region, wherein protruding

portions (see figure above) extending between a pair of opposite side surfaces of the mounting substrate are defined in the chip mounting surface of the mounting substrate, and the protruding portions are covered with the encapsulating layer (col 13, lines 4-6).

Allowable Subject Matter

2. Claims 5-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer Matisiak whose telephone number is 571-272-2639. The examiner can normally be reached on Business Days 9:30a-6:30p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 517-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEM

Douglas W. Owens

DOUGLAS W. OWENS
PRIMARY EXAMINER